1M BIT (128K WORD×8 BIT) CMOS MASK ROM
SILICON GATE CMOS

TC531000AP,TC531000AF

DESCRIPTION

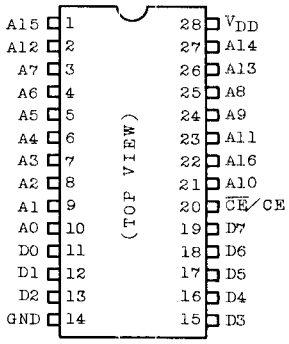
The TC531000AP/AF is a 1,048,576 bits read only memory organized as 131,072 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor, especially character generator. The TC531000AP/AF using CMOS technology is most suitable for low power applications where battery operation are required.

The TC531000AP/AF has one chip enable input $\overline{CE}$/CE, programmable for device selection.

FEATURES

- Single 5V Power Supply
- Access Time: 150ns (Max.)
- Power Dissipation
  - Operating Current: 40mA (Max.)
  - Standby Current: 20μA (Max.)
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- Fully Static Operation
- Programmable Chip Enable
- Package
  - Plastic DIP: TC531000AP
  - Plastic FP: TC531000AF

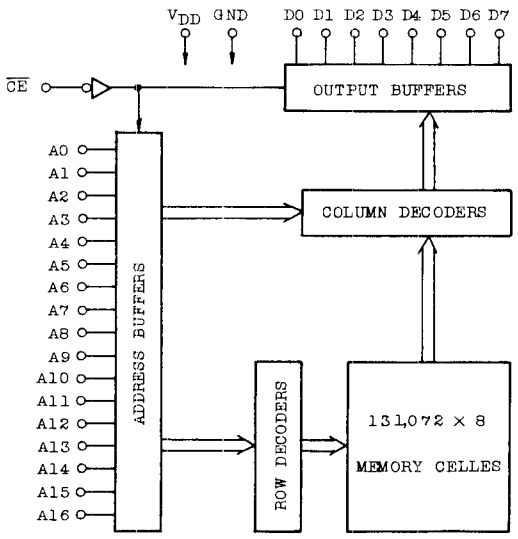
PIN CONNECTION



PIN NAMES

A0 ~ A16	Address Inputs
D0 ~ D7	Data Outputs
$\overline{CE}$/CE	Chip Enable Input
V_{DD}	Power Supply
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}	Input Voltage	−0.5 ~ V_{DD}	V
V_{OUT}	Output Voltage	0 ~ V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{OPR}	Operating Temperature	−40 ~ 70	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

Note: * Plastic FP

D.C. OPERATING CONDITIONS (Ta = −40 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = −40 ~ 70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	3.2	–	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}	–	2	mA
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD} and V_{IN} = 0V (V_{DD})	–	20	μA
I_{DD01}	Operating Current	V_{IN} = V_{IH} /V_{IL}, tcycle = 150ns	–	50	mA
I_{DD02}		V_{IN} = V_{DD}/0V, tcycle = 150ns	–	40	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f = 1MHz, Ta = 25°C	–	10	pF
C_{OUT}	Output Capacitance	f = 1MHz, Ta = 25°C	–	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

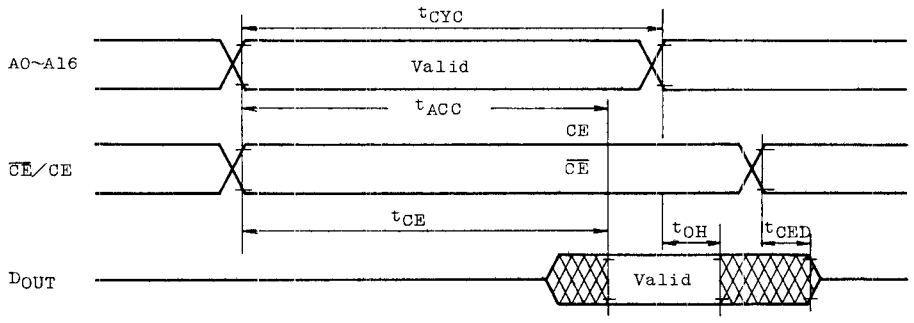
A.C. CHARACTERISTICS (V_{DD} = 5V ± 5V ± 10%, Ta = −40 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	150	—	ns
t_{ACC}	Access Time	—	150	ns
t_{CE}	Chip Enable Access Time	—	150	ns
t_{CED}	Output Disable Time	—	50	ns
t_{OH}	Output Hold Time	10	—	ns

AC TEST CONDITIONS

- Output Load : 100pF + 1TTL
- Input Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels Input : 0.8V, 2.2V
  Output : 0.8V, 2.0V
- Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



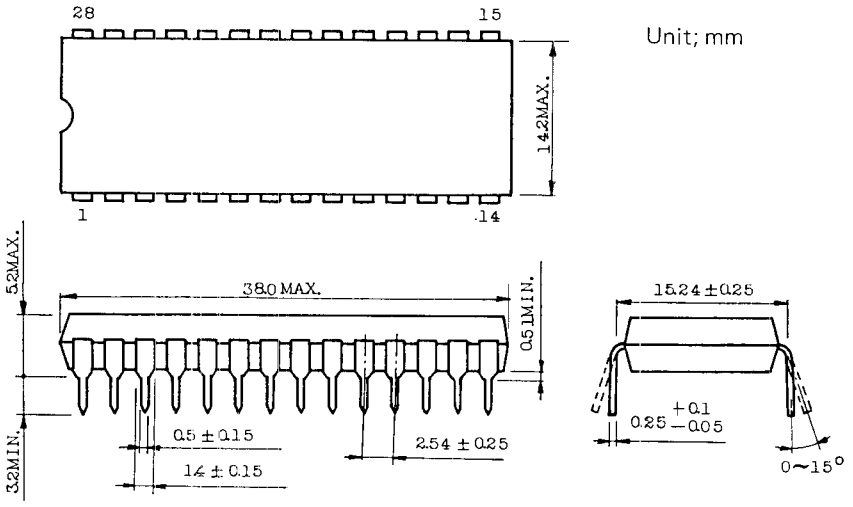
OPERATION MODE

MODE	$\overline{CE}$(CE)	A0 ~ 16	Outputs	Power
Read	L(H)	Valid	Data Out	Operating
Output Deselect	H(L)	*	High-Z	Standby

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

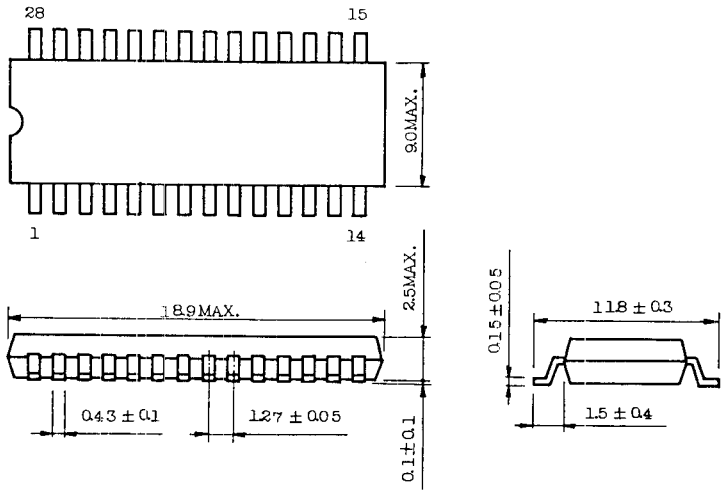
- OUTLINE DRAWINGS

Plastic DIP



NOTE: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

Plastic FP



NOTE: Each lead pitch is 1.27mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

NOTE: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserve the right, at any time without notice, to change said circuitry.